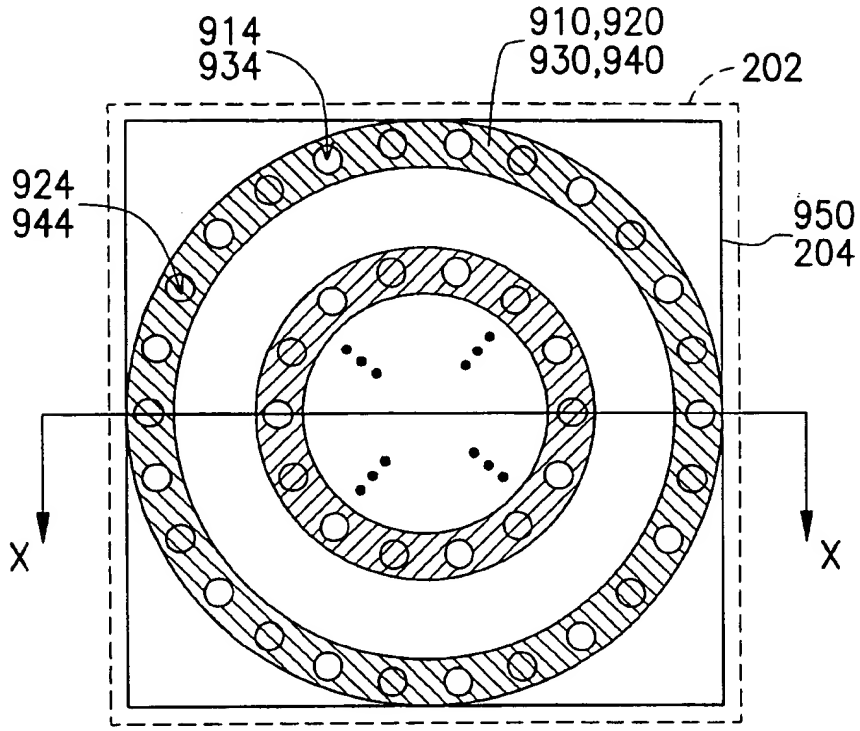
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950
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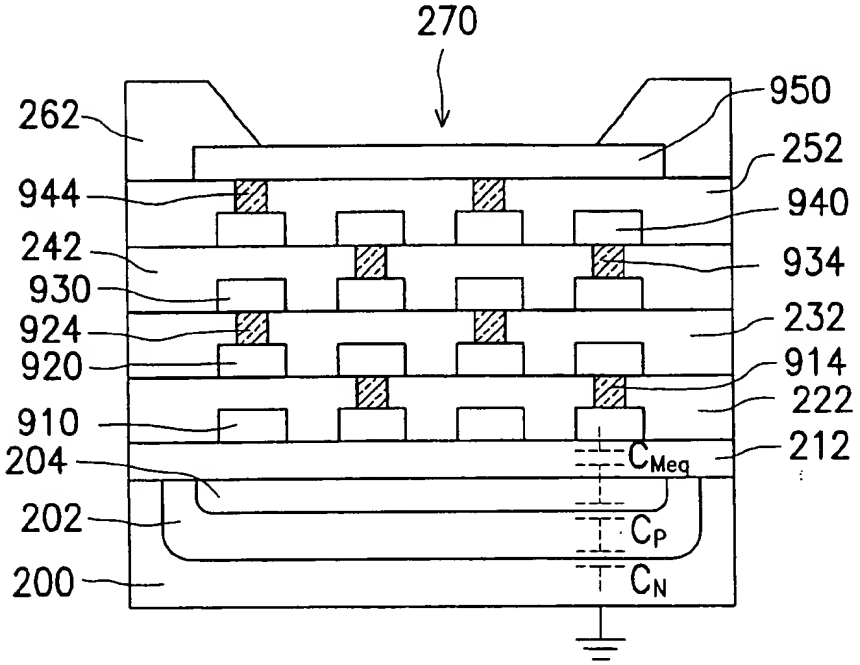
X
X

FIG. 9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944
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C_{Meq}
202
C_P
200
C_N

FIG. 10

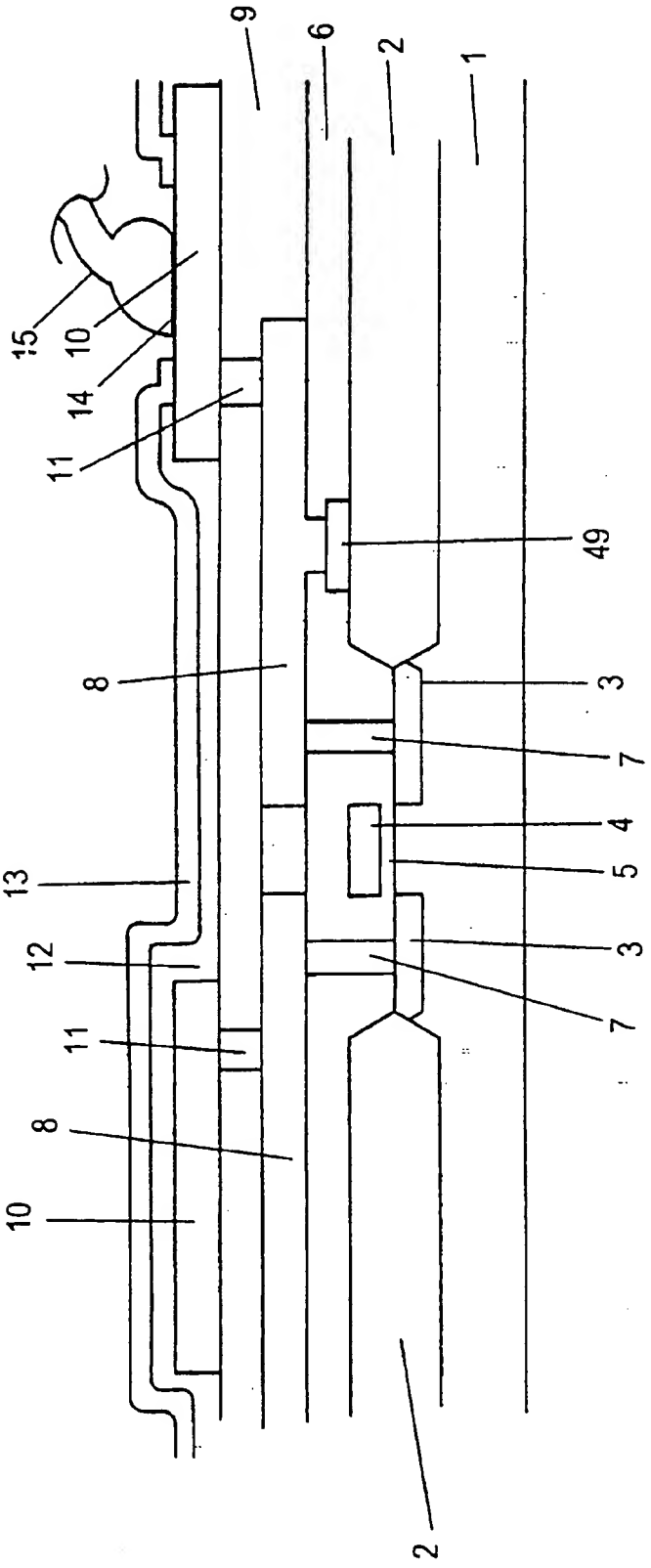

FIG. 1 PRIOR ART

US006362528B2

(12) **United States Patent**
Anand

(10) **Patent No.: US 6,362,528 B2**
(45) **Date of Patent: *Mar. 26, 2002**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventor: **Minakshisundaran Balasubramanian Anand**, Yokohama (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/915,398**

(22) Filed: **Aug. 20, 1997**

(30) **Foreign Application Priority Data**

Aug. 21, 1996 (JP) 8-219987

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52; H01L 29/40

(52) **U.S. Cl.** **257/758**; 257/784

(58) **Field of Search** 257/784, 758, 257/780, 786, 750, 751; 438/612, 634

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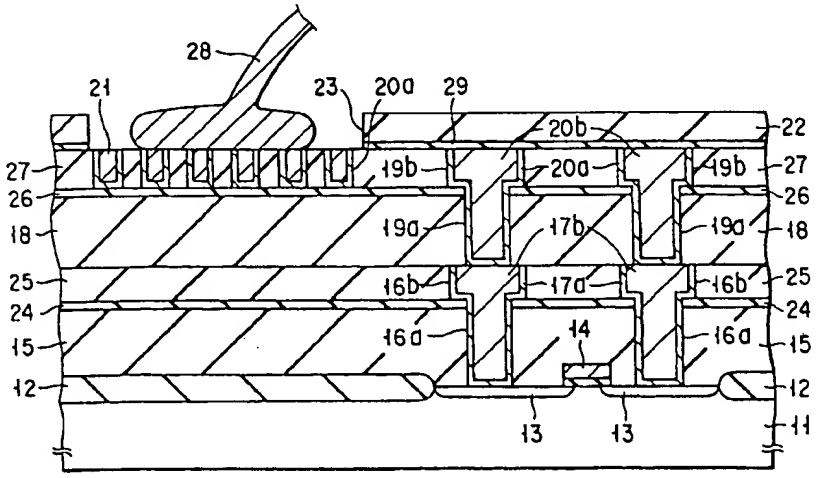
Primary Examiner—Phat X. Cao
(74) *Attorney, Agent, or Firm*—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

(57) **ABSTRACT**

In the present invention, the bonding pad is formed in a lattice-like shape. Directly underneath the passivation layer, the etching stopper layer is provided. An opening is made through the passivation layer and the etching stopper layer so as to expose the bonding pad. The cavity sections of the lattice-like shape of the bonding pad are filled with the insulating layer. The bonding wire is connected to the lattice-shaped bonding pad. With this structure, the bonding error of the device manufactured by the damascening process can be avoided.

12 Claims, 22 Drawing Sheets



US006303977B1

(12) **United States Patent**
Schroen et al.

(10) **Patent No.: US 6,303,977 B1**
(45) **Date of Patent: Oct. 16, 2001**

(54) **FULLY HERMETIC SEMICONDUCTOR CHIP, INCLUDING SEALED EDGE SIDES**

(75) Inventors: **Walter H. Schroen; Judith S. Archer,** both of Dallas; **Robert E. Terrill,** Houston, all of TX (US)

(73) Assignee: **Texas Instruments Incorporated,** Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/453,135**

(22) Filed: **Dec. 2, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/110,837, filed on Dec. 3, 1998.

(51) **Int. Cl.**[7] **H01L 29/80**

(52) **U.S. Cl.** **257/635**; 257/760; 257/702; 257/701; 257/758; 257/723; 257/620; 257/644; 257/788; 257/791; 257/792; 257/784; 257/786

(58) **Field of Search** 257/678, 700, 257/701, 758, 723, 730, 787, 786, 784, 774, 788, 791, 792, 768, 769, 760, 762, 773, 759, 668, 620, 632, 635, 644

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Primary Examiner—Alexander O. Williams
(74) *Attorney, Agent, or Firm*—Gary C. Honeycutt; Fred Telecky; Arthur I. Navarro

(57) **ABSTRACT**

A structure and method for forming a hermetically sealed semiconductor chip having an active and a passive surface and four edge sides, each edge side having only a single plane; said active surface having an integrated circuit including multiple deposited layers and a plurality of contact pads, said contact pads having bondable and non-corrodible surface; said deposited layers having exposed portions at said side edges; a protective overcoat impermeable to moisture overlying said integrated circuit; and a continuous sealant layer impermeable to moisture overlying all area of said four side edges, whereby said edge sides are sealed and said chip is rendered hermetic. Positioning a plurality of said chips on a support in a deposition apparatus and preferably using chemical vapor deposition or sputtering techniques, a layer, or a sandwich of layers, of moisture-impermeable material is deposited on all edge sides simultaneously while preventing deposition of said material on at least portion of the exposed active or passive surfaces.

12 Claims, 2 Drawing Sheets

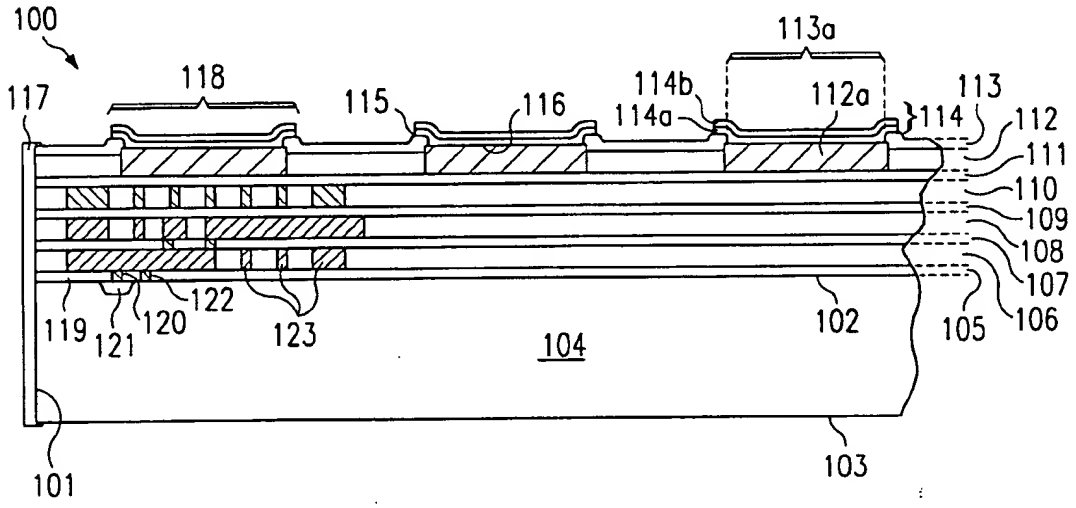

FIG. 19

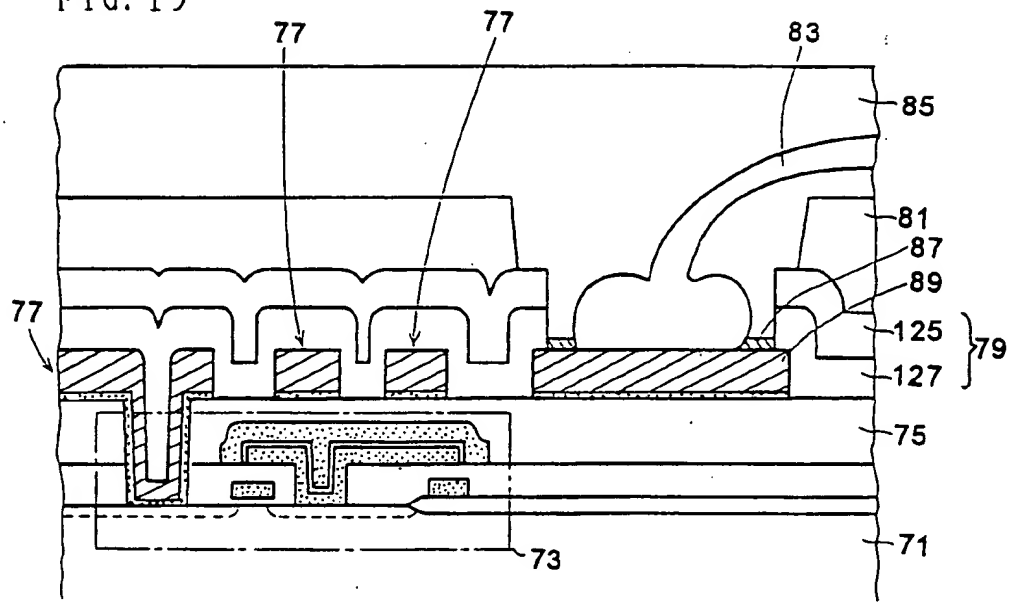
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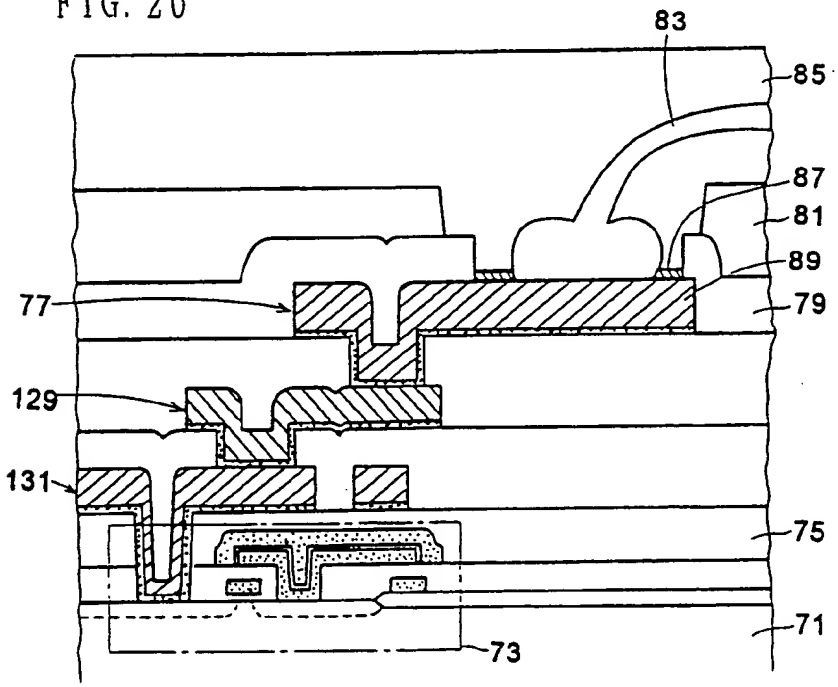
FIG. 20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US006261944B1

(12) **United States Patent**
Mehta et al.

(10) **Patent No.: US 6,261,944 B1**
(45) **Date of Patent: *Jul. 17, 2001**

(54) **METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING HIGH RELIABILITY PASSIVATION OVERLYING A MULTI-LEVEL INTERCONNECT**

(75) Inventors: **Sunil D. Mehta; Xiao-Yu Li**, both of San Jose, CA (US)

(73) Assignee: **Vantis Corporation**, Sunnyvale, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/200,395**

(22) Filed: **Nov. 24, 1998**

(51) **Int. Cl.**[7] **H01L 21/4763**

(52) **U.S. Cl.** **438/624**; 438/626; 438/631; 438/612

(58) **Field of Search** 438/626, 631, 438/632, 633, 634, 645, 646, 697, 698, 699, 758, 760, 782, 958, 624, 106, 612, 614, 617

(56) **References Cited**

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Primary Examiner—Charles Bowers
Assistant Examiner—Hsien-Ming Lee
(74) *Attorney, Agent, or Firm*—Brinks Hofer Gilson & Lione

(57) **ABSTRACT**

A semiconductor device having a high reliability passivation includes a planarization layer overlying a multi-level interconnect layer. The passivation layer has a planar surface upon which additional passivation layers are formed. Openings in the overlying passivation layers and the planarization layer expose bonding pads in the multi-level interconnect layer. In a process for fabricating the device, the planarization layer is preferably formed by dispensing a siloxane spin-on-glass (SOG) material onto the surface of the multi-level interconnect layer. The SOG is subsequently planarized to form a substantially planar surface.

23 Claims, 3 Drawing Sheets